IN THE SPECIFICATION

Please replace the titled as shown below.

~~MONOTONOUS~~ MONOTONIC UP-COUNTER IN AN INTEGRATED CIRCUIT

Please replace the paragraph beginning on page 1, line 6 as shown below.

The present invention relates to the field of integrated circuit counters. The present invention more specifically relates to the forming of an irreversibly ~~monotonous~~ monotonic up-counter.

Please replace the paragraph beginning on page 1, line 11 as shown below.

Currently, to form ~~monotonous~~ monotonic up-counters, fuse elements have to be used, which have the major disadvantage of causing a destructive programming often incompatible with a programming during operation of the integrated circuit containing the fuse element. Another example relates to EPROM or EEPROM memories, the manufacturing of which requires steps not directly compatible with a CMOS technology.

Please replace the paragraph beginning on page 1, line 26 as shown below.

The present invention aims at providing a one-time programming ~~monotonous~~ monotonic counter which overcomes the disadvantages of known solutions.

Please replace the paragraphs beginning on page 1, line 30 as shown below.

The present invention also aims at providing a ~~monotonous~~ monotonic increasing counter, the programming and the operation of which are compatible with applications requiring a linear counting.

To achieve these and other objects, the present invention provides an increasing ~~monotonous~~ monotonic counter over n bits formed as an integrated circuit, comprising:

Please replace the paragraphs beginning on page 2, line 13 as shown below.

According to an embodiment of the present invention, each counting cell is formed of a one-time programming memory cell, a ~~memorization~~ storage element of which is formed of at least one polysilicon resistor, programmable by irreversible decrease in its value.
The present invention also provides a method for controlling a counter, ~~consisting of~~ comprising causing a programming of a counting cell of a group of lower rank each time the parity controller of a group of immediately higher rank detects a parity.

Please replace the paragraph beginning on page 3, line 8 as shown below.

Fig. 7 shows an embodiment of an increasing ~~monotonous~~ monotonic counter according to the present invention;

Please replace the paragraph beginning on page 3, line 16 as shown below.

~~Same~~ The same elements have been designated with the same reference numerals in the different drawings. For clarity, only those elements that are necessary to the understanding of the present invention have been shown in the drawings and will be described hereafter. In particular, the different control signals of the counter and of its decoding elements have not been detailed and are within the abilities of those skilled in the art based on the following description. Further, the practical implementation of a polysilicon resistor usable in a counting cell according to the present invention involves conventional techniques known of those skilled in the art.

Please replace the paragraph beginning on page 5, line 4 as shown below.

In recent technologies, the use of polysilicon resistors is limited to resistors meant to ~~be run through~~ conduct, in operation, ~~by~~ currents smaller than 100 μA. For greater currents, a

diffusion resistor is generally used. Polysilicon is however preferred to a dopant diffusion, since the occurrence of stray capacitances with the substrate is avoided.

Please replace the paragraph beginning on page 9, line 29 as shown below.

The counting operation ~~consists of~~ comprises causing the irreversible decrease in the value of resistor Rp by applying a constraint current thereto. In read mode, the comparison of the voltage of a cathode with respect to a reference value enables determining whether the counting cell contains a state 0 or a state 1.